OLD DOCKET NO: DB3
NEW DOCKET NO: OSEM-DB3

IN RE APPLICATION OF: Braddock   Examiner: KANG

SERIAL NO: 09/636,484   GROUP ART UNIT: 2811

FILED: 08/10/00

TITLE: INTEGRATED TRANSISTOR DEVICES

TO: ASSISTANT COMMISSIONER OF PATENTS

37 CFR 1.132 DECLARATION OF DAVID BRADDOCK

I am the inventor, David Braddock:

1. There is no AlGaAs composition for which lattice matching exists with InP. Therefore, AlGaAs can not be grown epitaxially on InP with low defect densities. These facts are well known in the art in prior to 1997.

2. Even for a composition containing as low as one percent GaP, In_xGa_{1-x} P does not lattice match to an InP substrate. Therefore, InGaP cannot be grown epitaxially on InP with low defect densities. These facts were well known in the art in 1997.

3. The Passlack patent teaches using only AlGaAs or InGaP lattice matched to GaAs. The Passlack patent does not mention InP substrates. Passlack did not mention in the Passlack patent InP substrates presumably at least because Passlack knew that his AlGaAs and InGaP devices grown on an InP substrate would not produce a useful device.

4. It is now known that stoichiometric Ga2O3 is an *n type semiconductor*, not an insulator. It has room temperature residual n type conductivity on the order of 10^{16} per cubic centimeter. That conductivity is much larger than the conductivity of insulating materials used as gate insulators. Materials used as gate insulators generally have conductivities of *less than* 10^{12} per cubic centimeter. Accordingly, stoichiometric Ga2O3, which is what the Passlack patent teaches, is not useful for performing the function of a gate insulator.

5. At the time Passlack filed for his patent, he did not know that stoichiometric Ga2O3 had a relatively large residual conductivity. I speculate that Passlack filed for the Passlack patent assuming that residual conductivity of Ga2O3 was caused by defects, vacancies, or impurities and therefore he thought that conductivity could potentially be reduced to a level at which his Ga2O3 would be commercially useful as a gate insulator.

6. The devices disclosed in the Passlack patent are not commercially useful. Ga2O3 does have a relatively large conductivity, which is one reason why the devices disclosed in the Passlack patent are not commercially useful.

7. The Passlack patent does not disclose a gate insulator. Instead, the Passlack patent discloses:

> The FET includes a *stoichiometric Ga2O3 gate oxide layer* positioned on upper surface of a compound semiconductor wafer structure. [Col. 2 lines 45-47; emphasis supplied.]

8. There is no motivation in the art to substitute InP for the substrate used by Passlack, for two reasons. First, there is no specific teaching of suggestion of such a modification of Passlack's teachings. Second, it is well known that such a substitution would prevent epitaxial low defect growth of either one of the AlGaAs and InGaP epitaxially grown materials disclosed in the Passlack patent.

9. Second, Passlack's stoichiometric Ga2O3 does not respond to the limitation defined in claims 36 and 38 of "a gate insulator structure." The first paragraph of the section of the specification of this application describing my invention defines the "gate insulator structure" recited in claims 36 and 38 as both electrically insulating and comprising at least two layers. That paragraph states in part:

> The present invention provides, among other things, a self-aligned enhancement mode metal-oxide-compound semiconductor FET. The FET includes *a gallium oxygen insulating structure that is composed of at least two distinct layers*. The *first layer is* most preferably more that 10 angstroms thick but less that 25 angstroms in thickness and *composed substantially of gallium oxygen compounds including but not limited to stoichiometric Ga_2O_3 and Ga_2O, and possibly a lesser fraction of other gallium oxygen compounds.* The *upper insulating layer in the gallium oxide insulating structure* is composed of an insulator that does not intermix with the underlying gallium oxygen insulating structure. This upper layer must possess excellent insulating qualities, and is most typically composed of gallium oxygen and a third rare earth element that together form a ternary insulating material. *Therefore the entire gallium oxide rare earth gate insulator structure is composed of at least two layers* and may contain a third intermediate graded layers that consists of a mixture of the upper insulating material and the gallium oxygen compounds that compose the initial layer.

10. Please note that I wrote the specification without advise of counsel, which explains in part the reference to two layers as "first layer" and "upper insulating layer" to the extent that that lack of clarity and any other descriptions that lack complete clarity cause the panel any confusion.

11. The specification contains specific references to "gate insulator structure" or the equivalent "gate insulating structure" all of which are consistent with a multi layer structure that is insulating to the extent necessary to form a useful gate insulator. See the recitations:

> A refractory metal gate electrode is preferably positioned on the upper surface of the gate insulator structure layer. [Page 5 lines 10-12.]

> Together the lower gallium oxide compound layer and the second insulating layer form a gallium oxide gate insulating structure. [Abstract.]

> The gallium oxide gate insulating structure and underlying compound semiconductor gallium arsenide layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14). [Abstract.]

12. Third, the Passlack patent does not disclose a gate insulator. The teachings of the Passlack patent do not enable one skilled in the art to form a structure containing a commercially useful device because the conductivity of the *stoichiometric Ga2O3 gate oxide layer* taught by Passlack is too high to be useful, the Passlack patent does not teach one or ordinary skill in the art this fact, and the Passlack patent does not teach one of ordinary skill in the art how to make a gate insulating structure having low enough conductivity to be useful.

2. **Argument (Reasoning) Respecting How Claim 38 Complies with 35 USC 112**

13. In rejecting claim 38 for lack of support, the examiner states that:

> The specification does not support the limitation "said transistor is integrated together with similar and complementary transistor devices to form complementary metal-oxide-compound semiconductor integrated circuit." [Office action page 4 lines 3-5.]

14. In reply, I disagree. I point out that the recited limitation is disclosed in the following locations in my application:

15. The last sentence of the abstract states that:

> Multiple devices are then positioned in proximity and the appropriate interconnection metal layers and insulators are utilized in concert with other passive circuit elements to form a integrated circuit structure.

16. The consider the abstract as part of my specification.

17. The specification in the field of the invention section states (page 1 lines 3-9) "The present invention pertains to ... fabrication of said structures and the ultra large scale integration of said transistors." Ultra large scale integration implies to one skilled in the art the use of complementary circuit architectures.

18. In the discussion of the background section (page 1 lines 11-13) I identify a problem addressed by the invention, which is that "The gallium arsenide and indium phosphide integrated circuit industry has been limited without a technology that simultaneously allows the integration of complementary field effect transistor devices and transistors with low gate leakage currents." Thus, I clearly identify the invention with integration of complementary field effect transistor devices and transistors.

19. I specifically associated the application for this invention with large scale architectures, stating that "What is also needed are new and improved self-aligned compound semiconductor MOSFETs for use in complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for low power/high performance complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which offer the design

flexibility of complementary architectures. "

20. In the specification of the invention section, I state that:

> Thus, new and improved compound semiconductor devices and methods of fabrication are disclosed. The new and improved self-aligned enhancement mode metal-oxide-compound semiconductor heterostructure field effect transistors enable stable and reliable device operation, provide optimum compound semiconductor device performance for low power/high performance *complementary circuits* and architectures, keep interconnection delay in ULSI under control, and provide optimum efficiency and output power for RF and microwave applications as well as for digital integrated circuits that require very high integration densities. [Page 9 lines 19-26.]

21. Furthermore, original claim 37 recited "integrated together with similar and complementary transistor devices to form complementary metal-oxide compound semiconductor integrated circuits."

22. Finally, Fig. 2 element 112 states "Provide Interconnection Means for the Formation of an Integrated Circuit" thereby conveying the concept of using multiple instances of a structure defined by the claimed invention.

23. Therefore, I clearly disclosed that this invention was directed for use in integrated circuits including similar instances of the claimed transistor structure and in circuits using complementary (which means p and n type) devices.

24. I swear under penalty of perjury that the foregoing is true and correct.

11/13/2002
DATE

DAVID BRADDOCK

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